

ATTORNEY DOCKET NO. CN020002 (STNX01-20002)
U.S. SERIAL NO. 10/500,620
PATENTREMARKS

Claims 1, 3 and 5-20 are pending in the application.

Claims 1, 3, 5, 6 and 8-20 have been rejected.

Claims 1, 5, 6 and 8-14 are amended.

Claim 7 is objected to.

Reconsideration of the Claims is respectfully requested in light of the above amendments and the following remarks.

I. ALLOWABLE SUBJECT MATTER

The Office Action indicates that Claim 7 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant thanks the Examiner for this indication of allowable subject matter, but elects not to rewrite Claim 7 at this time.

II. REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 3, 5, 6, and 8-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe (U.S. Patent No. 5,319,798) in view of Cairns (U.S. Patent No. 5,794,131). Claims 15-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe in view of Cairns and further in view of Hung et al. (U.S. Patent No. 6,370,361). The rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If

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the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), viz., (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

The Applicant respectfully submits that the combination of cited references fails to teach or suggest all the claim limitations of independent Claim 1. Specifically, Claim 1 has been amended to recite, "wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state and receiving a modulation signal." (underlining supplied).

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Claim 1 is being amended to clarify that the digital synthesizer driven phase locked loop (in a modulation state) receives a modulation signal. For ease of reference, Paragraph [0025] of the Applicant's published application is set forth below:

[0025] Thereto, mode detector 41 detects the transceiver, during a first time-interval, being in a transmitting mode, for example via a coupling not shown to transmitter part 2, and/or for example by making a calculation, with said first and second time slots being standardized, and informs processor/memory system 42, which instructs modulation signal generator 45 to generate a modulation signal (for example in response to an audio signal originating from a man-machine-interface not shown and coupled to processor/memory 42) and instructs control signal generator 43 to generate a first control signal. In response to this first control signal, switch 32 supplies said modulation signal originating from modulation signal generator 45 to DDS 24, and switch 11 couples first filter 12 to VCO 10, with first filter 12 for example being a loop filter for improving the PLL function and for example having a bandwidth which is equal to or a little larger than the (occupied) bandwidth of the modulation signal. DDS 24 receives a multiplied clock signal comprising clock pulses via multiplier 31 and clock generator 30, and receives said modulation signal. At the hand of DDS 24, any signal including complex waveforms can be generated by defining one or more of at least three parameters being frequency, phase and amplitude respectively. These three parameters respectively can be controlled by frequency control words (with frequency modulation being achieved before/in phase accumulator 23), phase control words (with phase modulation being achieved between/in phase accumulator 23 and sine shaper 22) and amplitude control words (with amplitude modulation being achieved between/in sine shaper 22 and D/A converter 21) respectively. Said modulation signal manipulates one or more of these control words, and as a result, DDS 24 generates a modulated reference signal which is supplied to PLL 10-15, which, via phase detector 14 and first filter 12 and switch 11 and VCO 10, with divider 15 being in a feedback loop, locks this modulated reference signal. The locked modulated reference signal is supplied via switch 5 to transmitter part 2, due to switch 5, for example in response to said first control signal or a further control signal originating from controller 40, connecting VCO 10 with transmitter part 2. Transmitter part 2, for example comprising an auto gain controller, a filter and a power amplifier, supplies an amplified, filtered and gain controlled locked modulated reference signal to switch 3 and therefore provides a direct digital RF modulation. Switch 3 supplies this signal to antenna 1, due to switch 3, for example in response to said first control signal or a further control signal originating from controller 40 via a coupling not shown, connecting transmitter part 2 with antenna 1. So, during this first time-interval, the

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transceiver is in a transmitting mode, and the DDS driven PLL 24,10-15 is in a modulating state.

As described above, the digital synthesizer uses the modulation signal to generate a modulated reference signal, which is supplied to the phase locked loop. The locked modulated reference signal may provide for direct digital RF modulation.

In distinct contrast to the Applicant's claimed modulation signal, Watanabe relates to a frequency control signal supplied from a control portion of the radio transceiver to a frequency divider of the PLL synthesizer for switching the carrier frequency and is limited to an OFF period of the carrier transmitting/receiving period. Watanabe, Abstract. Accordingly, the frequency control signal of Watanabe is not a modulation signal and is not received during a modulation state.

With regard to Cairns, the TXIF signal is used to provide "fine" control over the transmit frequency of the synthesizer 300. Thus, the TXIF signal is not a modulation signal. Also, the DATA, CLOCK, and STROB₁₃₃ of Cairns are used to control the synthesizer 300. Cairns, Col. 13, lines 54-63. According, none of the DATA, CLOCK, and STROB₁₃₃ of Cairns appears to provide a modulation signal as claimed in Claim 1.

Thus, the Applicant respectfully submits that both Watanabe and Cairns (individually or any motivated combination thereof) fail to describe, teach or suggest "wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state and receiving a modulation signal." (underlining supplied).

Independent Claims 5 and 8-14 also have been amended to recite limitations analogous to the novel limitations emphasized above in traversing the rejection of Claim 1 and, therefore, also are patentable over the combination of cited references. Therefore, the Applicant respectfully submits that independent Claim 1 (and the other independent claims) is patentable over the cited references.

With respect to the rejection of dependent Claims 15-20 over Watanabe, Cairns, and Hung, for the same or similar reasons set forth above, and because the cited portion of Hung fails to cure the noted deficiency in the cited references, these claims are also patentable.

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Accordingly, the Applicant respectfully requests withdrawal of the § 103(a) rejections of Claims 1, 3, 5, 6, and 8-20.

III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

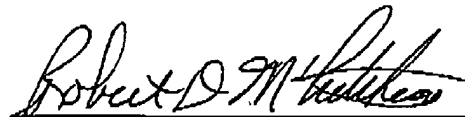
If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *rmccutcheon@munckcarter.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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